ABSTRACT OF THE DISCLOSURE

A nonvolatile semiconductor memory device having a small layout area includes a memory cell array in which a plurality of memory cells are arranged in a row direction and a column direction, wherein each of the memory cells includes a source region, a drain region, a channel region between the source region and the drain region, a word gate and a select gate disposed to face the channel region, and a nonvolatile memory element formed between the word gate and the channel region, wherein the wordline-and-selectline-driver-section includes a plurality of unit wordline-and-selectline-driver-sections, and wherein each of the unit wordline-and-selectline driver sections drives the select gates and the word gates of the memory cells in each row at a single potential.